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(54) Stacked multichip integrated semiconductor device including feed-through connections

(57) The integrated semiconductor device (1) includes a first chip (4) of semiconductor material having first, high-voltage, regions (12-17) at a first high-value voltage; a second chip (6) of semiconductor material having second high-voltage regions (31, 33) connected to the first voltage; and a third chip (5) of semiconductor material arranged between the first chip and the second chip and having at least one low-voltage region (21) at a second, low-value, voltage. A through connection region (22) is formed in the third chip and is connected to the first and second high-voltage regions; through insulating regions (23-25) surround the through connection region and insulate it from the low-voltage region.

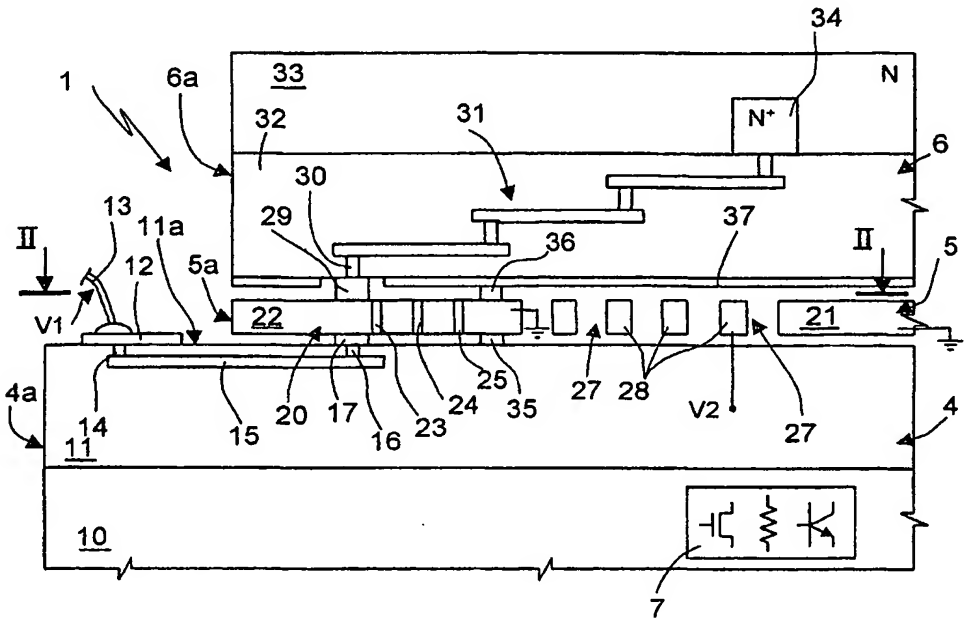


Fig.1

EP 1 225 635 A2

Description

[0001] The present invention relates to an integrated semiconductor device including high-voltage interconnections passing through low-voltage regions.

[0002] As is known, passage of high-voltage interconnections on integrated circuits of semiconductor material, such as silicon, already at voltages of over 100 V requires the adoption of sophisticated solutions at layout and process levels to overcome the effects of the charge induced in the semiconductor material and of charge movements in the dielectrics. In fact, in these situations, malfunctioning may occur in the integrated circuits.

[0003] The simplest solutions currently implemented to overcome the above-mentioned effects comprise providing field plates, i.e., electrostatic shields of semiconductor material, typically doped polycrystalline silicon or metal, extending between the interconnection lines and the areas to be protected. These field plates modify the electric field existing in critical areas, such as the insulations for positive-potential interconnections and N^- doped areas for negative-potential interconnections.

[0004] In addition, the thickness of the dielectric layer on which the interconnections extend increases as the voltages carried by the interconnections increase. Beyond a certain voltage value, however, the thickness becomes considerable and not always compatible with present processes and dimensional requirements. Consequently, whenever possible, the interconnections are made in "bridge" fashion, using bonding wires.

[0005] Particular problems are encountered in case of high voltages supplied to parts of devices formed on various wafers some of which are low-voltage ones. In this case, in fact, the various wafers house different parts of the device which are to be electrically and mechanically connected through bonding structures.

[0006] In particular, in these devices, the various parts are connected by interconnections of metal and strongly doped silicon which must be able to withstand high voltages and confine them so as to prevent the high electric fields associated thereto from damaging or hindering proper operation of the low-voltage parts.

[0007] The aim of the present invention is to overcome the limitations of the prior art by providing an interconnection system in a device formed in various wafers and including high-voltage parts and low-voltage parts.

[0008] According to the present invention, an integrated semiconductor device is provided, characterized by:

a first chip of semiconductor material having first high-voltage regions at a first, high-value, voltage;
a second chip of semiconductor material having second high-voltage regions at said first, high-value, voltage;
a third chip of semiconductor material extending between said first and second chip and having at least one low-voltage region at a second, low-value, voltage;
a through connection region formed in said third chip and connected to at least one of said first and second high-voltage regions; and
through insulating regions surrounding and insulating said through connection region.

[0009] For a better understanding of the present invention, preferred embodiments thereof are now described, purely to provide non-limiting examples, with reference to the attached drawings, wherein:

- Figure 1 illustrates a longitudinal section of a data storage device;
- Figure 2 is a cross-sectional view of the device of Figure 1, taken along line II-II;
- Figure 3 shows a longitudinal section of the device of Figure 1, taken along a sectional plane parallel to that of Figure 1;
- Figure 4 is a cross-sectional view of the device of Figure 3, taken along the line IV-IV;
- Figure 5 is a perspective sectional view of a different embodiment of the device of Figure 1; and
- Figure 6 is a perspective sectional view of the device of Figure 5, taken along a sectional plane parallel to that of Figure 5 and showing a different type of connection.

[0010] As shown in Figure 1, a data-storage device 1 comprises three chips arranged on each other; namely, a bottom chip 4, which is supplied by a first, high-value, voltage V1 (higher than 100 V; for instance, 300, 500 or 1000 V), an intermediate chip 5 set, as a whole, at a low voltage, and a top chip 6 which must be supplied with the first voltage. The bottom chip 4 has larger dimensions than the intermediate chip 5 and the top chip 6, and projects laterally with respect to the other two at least on one side 4a (on the left in Figure 1). In practice, the intermediate chip 5 and the top chip 6 have a respective side 5a and 6a which are mutually aligned and are set back with respect to the corresponding side 4a of the bottom chip 4.

[0011] In detail, the bottom chip 4 houses the low-voltage control circuitry 7 (schematically represented in Figure 1 by electronic components) and comprises a first substrate 10 of semiconductor material (typically silicon) connected to ground. A first insulating layer 11 of dielectric material extends on the first substrate 10 of the bottom chip 4 and houses various metal levels (as may be better seen in Figure 3); it moreover carries, on its surface 11a, in the area of the bottom chip 4 that projects with respect to the chips 5, 6, a pad region 12 connected, through an electric wire 13 and discrete components positioned on a printed-circuit card (not shown), to a high-voltage generator (not shown either), for example generating a voltage of 1000 V.

[0012] The pad region 12 is connected, through a first via 14, to a first end of a metal connection region 15

extending inside the first insulating layer 11 formed, for instance, in the last metal level so as to be set as far as possible away from the first substrate 10 of the bottom chip 4. A second end of the metal connection region 15 is connected, through a second via 16, to a first contact region 17, of metal, formed on the surface 11a of the first insulating layer 11, beneath the intermediate chip 5. Underneath the metal connection region 15 no components are present so as to prevent any malfunctioning and damage caused by the high electric field generated by the metal connection region 15.

[0013] The intermediate chip 5 is formed by a body 21 of semiconductor material set at a second voltage of a low value, for example ground. The body 21 houses a micromechanical storage structure including a suspended mobile structure 27 and a connection structure 20.

[0014] The suspended mobile structure 27 is set at at least one third voltage V2, with an absolute value lower than the first voltage V1 and different from the second voltage (for example, the third voltage is 3 to 10 V).

[0015] The connection structure 20 has the aim of transferring the first voltage from the bottom chip 4 to the top chip 6, and comprises a through connection region 22, which is insulated from the rest of the body 21 by three insulation regions 23, 24 and 25. The through connection region 22 is arranged on and in direct electrical contact with the first contact region 17. The insulation regions 23, 24, and 25, for example of silicon dioxide, are of the through type (and thus extend throughout the thickness of the intermediate chip 5), and each of them comprises (Figure 2) a semicircular portion 23a, 24a, 25a and two rectilinear portions 23b, 24b, 25b. The semicircular portions 23a, 24a, 25a of the three insulation regions 23-25 are concentric and partially surround the through connection region 22. The rectilinear portions 23b, 24b, 25b are parallel to each other and extend tangentially from the two ends of the respective semicircular portion 23a, 24a, 25a, as far as the side 5a of the intermediate chip 5, so that the insulation regions 23-25 are U-shaped as seen in top view.

[0016] The suspended mobile structure 27, for example a translating microactuator, comprises a plurality of suspended regions 28 connected to the rest of the body 21 of the intermediate chip 5, in a per se known manner, by supporting arms (not shown).

[0017] A second contact region 29, preferably of metal, extends on and in direct electrical contact with the through connection region 22, and is vertically aligned to the first contact region 17. The second contact region 29 is connected, through a third via 30, to a first metal line structure 31 having a plurality of metal levels (here, three) that is formed in a second insulating layer 32 of the top chip 6. The second insulating layer 32 covers the bottom side of a second substrate 33 belonging to the top chip 6. The second substrate 33 must be biased at the first voltage and therefor houses an enriched contact region 34.

[0018] The top chip 6 houses a control circuit and carries a matrix of electron beam emitters, not shown and forming a probe of an atomic-resolution memory (not illustrated).

[0019] First and second spacer regions 35, 36 are respectively arranged between the bottom chip 4 and the intermediate chip 5, and the intermediate chip 5 and the top chip 6. The spacer regions 35, 36 are of insulating material if the substrate 33 of the top chip 6 is biased at a voltage of over 300 V. Alternatively, for lower voltages, the spacer regions 35, 36 may be formed of the same metal material of respectively the first contact region 17 and the second contact region 29. The second spacer regions 36, arranged between the intermediate chip 5 and the top chip 6, advantageously surround and seal the area of the top chip 6 containing the emitter matrix, as well as the area of the intermediate chip 5 comprising the suspended mobile structure 27. The gap between the top chip 6 and the intermediate chip 5 is, for example, 1.5 μm and is filled with air, nitrogen, or some other inert gas, or is set in vacuum conditions.

[0020] An insulating material layer 37 covers the bottom surface of the top chip 6.

[0021] Figures 3 and 4 show portions of the device 1 accommodating the electrical signal connections between the emitter matrix housed in the top chip 6 and the components of the circuitry 7, housed in the bottom chip 4. In particular, the electrical connections have the aim of bringing the electrical signal to the circuitry 7, uncoupling it from the first voltage V1 (high-value biasing voltage).

[0022] Figure 3 shows a second metal line structure 40, formed inside the first insulating layer 11 of the bottom chip 4 using three metal levels and connecting a component of the circuitry 7, formed in the first substrate 10, to a third contact region 41 arranged on the surface 11a of the first insulating layer 11.

[0023] Figure 3 shows the suspended mobile structure 27 of the intermediate chip 5. In addition, Figure 3 shows a signal connection structure 42 formed inside the body 21. The signal connection structure 42 comprises a cylindrical region 43, of silicon, extending for the entire thickness of the intermediate chip 5 and surrounded by three insulation rings 44, 45 and 46 which are concentric to each other and to the cylindrical region 43. In particular, the insulation ring 44 surrounds the cylindrical region 43, and the insulation rings 44-46 delimit between them a first and a second annular semiconductor region 47, 48 (see also Figure 4). The second annular semiconductor region 48 (the outermost one) is in direct electrical contact with the third contact region 41. The insulation rings 44-45, the annular semiconductor regions 47, 48, and the cylindrical region 43 form a capacitive element 50 including two series capacitors, of which the cylindrical region 43 and the annular semiconductor regions 47, 48 form the plates, and the insulation rings 44-45 form the intermediate dielectric. The insulation ring 46 (the outermost one) insulates the capacitive

element 50 from the rest of the body 21.

[0024] The cylindrical region 43 is in direct electrical contact with a fourth contact region 51, of metal material and arranged between the intermediate chip 5 and the top chip 6. The fourth contact region 51 is electrically connected to a fourth metal line structure 52 having a plurality of levels (here, three) formed in the second insulating layer 32 of the top chip 6.

[0025] Thereby, electrical signals may be exchanged between the emitter matrix (not shown) formed in the top chip 6 and the circuitry 7 integrated in the bottom chip 4, with DC uncoupling via the capacitive element 50. In addition, the body 21 of the intermediate chip 5 can be electrically connected to ground even in the area immediately outside the insulation ring 46, notwithstanding the high voltage present in the cylindrical region 43 (for example, 300 or 1000 V).

[0026] In addition, thanks to the shape of the through portion 22 and to the absence of electronic components beneath the metal connection region 15, the device 1 has no structures that are to be kept at a low voltage (or even at ground voltage) above or below the metal connection region 15; consequently, the high electric field generated by the metal connection region 15 does not in any way jeopardize operation of any of the parts of the device 1.

[0027] The device 1 is manufactured as described hereinafter. Initially, the circuitry 7 is formed in a first wafer of semiconductor material, which is to form the bottom chip 4. Next, in a known way, the first insulating layer 11, the metal connection region 15, the third metal line structure 40, the pad 12, and the contact and spacer regions 17, 41 and 35 are formed. Either simultaneously or separately, deep trenches are formed in a second wafer of semiconductor material which is to form the intermediate chip 5, and are filled with insulating material to form the insulation regions 23-25 and the insulation rings 44-46. Deep trenches are moreover formed for defining the suspended mobile structure 27. The second wafer is turned upside down and bonded to the first wafer, and then its thickness is reduced until the insulation regions 23-25 and the insulation rings 44-46 are reached from the rear. Either simultaneously or separately, a third wafer, which is to form the top chip 6, is processed in such a way as to form the emitter matrix, the second insulating layer 32, the second and fourth metal line structures 31, 52, as well as the contact and spacer regions 29, 51, 36. Next, the third wafer is turned upside down and is bonded to the second wafer, and the wafers are cut.

[0028] Figures 5-6 show a different embodiment of the device 1 illustrated in Figures 1-4, useful when the gap between the intermediate chip 5 and the top chip 6 is small (for example, 1.5 μm) and the voltage of the substrate 33 of the top chip 6 is high, so that an electric field greater than or equal to 200 V/μm is present. In fact, in the absence of adequate measures, this field value could cause the suspended mobile structure 27 to collapse.

[0029] To reduce this risk, according to Figures 5-6, an electrostatic-shield structure 70 is provided such as to reduce the area of the equivalent capacitor formed by the top chip 6 and the intermediate chip 5, which face each other, and by the dielectric (air or another gas) enclosed between them.

[0030] In detail, Figure 5 shows a data-storage device 60 having a general structure similar to that of the data-storage device 1 of Figure 1. Consequently, the parts of the device 60 of Figure 5 that are the same as those of the device 1 of Figures 1-4 are designated by the same reference numbers and will not be described any further.

[0031] In Figure 5, a medium-to-high voltage (for example 300 V) is carried by a pad 12 arranged on the bottom chip 4, through a metal connection region 15, to the first contact region 17 extending on the surface 11a of the first insulating layer 11.

[0032] The intermediate chip 5 houses, in the connection portion 20, an insulation structure 63 equal to the connection portion 20 of Figures 1 and 2, and hence comprising a through connection region 22, insulated from the rest of the body 21 by three insulation regions 23, 24 and 25. The through connection region 22 is arranged on, and is electrically connected to, the first contact region 17. In addition, it is electrically connected to the second contact region 29. Consequently, the through connection region 22 and the first and second contact regions 17, 29 are at a high voltage (equal to the voltage applied to the pad 12); the body 21 of the intermediate chip 5, outside the insulation regions 23, 24 and 25, is at a low voltage (ground), and the conductive regions between adjacent pairs of insulation regions 23, 24 and 25 are at intermediate voltages between the high voltage and the low voltage.

[0033] The top chip 6 of Figure 5, of which only the second insulating layer 32 and the second metal line structure 31 are shown, has the same structure as in Figure 1, except for the fact that it supports an electrostatic-shield structure 70.

[0034] The electrostatic-shield structure 70 comprises a dielectric layer 71 and a conductive layer 72. The dielectric layer 71 is, for example, of a polymer, such as polyimide, extends on the bottom side of the top chip 6, and has a thickness of preferably 3-5 μm. The conductive layer 72 covers the surface of the dielectric layer 71 facing the intermediate chip 5, is preferably of metal (for example, aluminum), and has a thickness of, for instance, 0.5-1 μm.

[0035] The conductive layer 72 is electrically connected to the intermediate chip 5 by bump regions 73 of metal that extend between the conductive layer 72 of the electrostatic shield 70 and the intermediate chip 5. Specifically, the bump regions 73 are in direct electrical contact with the body 21 of the intermediate chip 5, and thus maintain the conductive layer 72 at the voltage of the intermediate chip 5 (i.e., ground voltage).

[0036] Thereby, the electrostatic-shield structure 70

extends between the top chip 6, at a high voltage, and the intermediate chip 5, and in particular the suspended mobile structure 27, so reducing the risk of collapse of the suspended mobile structure 27 towards the top chip 6.

[0037] The electrostatic-shield structure 70 is preferably formed by depositing and defining a dielectric material layer (for example, polyimide) on the surface of the second insulating layer 32 of a wafer that is to form the top chip 6 and in which the envisaged structures, such as the emitter matrices and the first metal line structures 31, are already provided. Thereby, the shield layer 71 is formed. Next, a metal layer is deposited and defined to form the conductive layer 72. Then, the bump regions 73 and the second contact regions 29 are formed in a known way, for example by making a negative mask of sacrificial material provided with openings where the bump regions 73 and the second contact regions 29 are to be formed, by depositing metal, and by removing the excess metal and subsequently the sacrificial material.

[0038] Figure 6 shows the electrostatic-shield structure 70 in the area of the signal connections between the top chip 6 and the circuitry 7 integrated in the bottom chip 4, described in detail with reference to Figures 3 and 4.

[0039] Finally, it is evident that modifications and variations may be made to the devices described herein, without thereby departing from the scope of the present invention.

[0040] For example, the invention is applicable to any device including three chips arranged on top of one another and bonded together, wherein a high voltage (i.e., higher than 100 V) has to be brought between two end chips, whereas the intermediate chip is set at a low voltage, regardless of the type of microstructure and/or circuit made in the chips. In addition, the number of insulation regions 23-25 or of insulation rings 44-46 may be any whatsoever, with a minimum of two, according to the high voltage to be transferred and compatibly with the need to limit the overall dimensions associated thereto. Furthermore, the connection structure 20 shown in Figures 1 and 2 and the signal connection structure 42 shown in Figures 3 and 4 may even not coexist in the same device, should only one of them be required.

Claims

1. An integrated semiconductor device (1; 60) **characterized by**:

   a first chip (4) of semiconductor material having first high-voltage regions (12-17) first, high-value, voltage;
   a second chip (6) of semiconductor material having second high-voltage regions (31, 33) at said first, high-value, voltage;
   a third chip (5) of semiconductor material extending between said first and second chip and having at least one low-voltage region (21) at a second, low-value, voltage;
   a through connection region (22; 43) formed in said third chip and connected to at least one of said first and second high-voltage regions; and
   a through insulating region (23-25; 44-46) surrounding said through connection region and insulating said through connection region from said low-voltage region.

2. The device according to Claim 1, wherein said through insulating region (23-25; 44-46) comprises at least one first insulating region (24; 45) surrounding said through connection region (22; 43) and a second insulating region (25; 46) surrounding at a distance said first insulating region, a first semiconductor region (48) extending between said first and second insulating regions.

3. The device according to Claim 2, wherein said through insulating region (23-25; 44-46) further comprises a third insulating region (23; 44) extending between said through connection region (22; 43) and said first insulating region (24; 45), a second semiconductor region (47) extending between said third and first insulating regions.

4. The device according to any of the foregoing claims, wherein said first chip comprises a first substrate (10) of semiconductor material; a first insulating layer (11) on top of said first substrate; and an external connection structure (12-17) extending at least partially on top of said first insulating layer and comprising a first contact region (17) formed on top of said first insulating layer (11) and in electrical contact with said through connection region (22), and wherein said second chip (6) comprises a second substrate (33) of semiconductor material; a second insulating layer (32) on top of said second substrate; and a first connection line structure (31) formed inside said second insulating layer; a second contact region (29) extending between said second insulating layer and said third chip (5) and being in electrical contact with said first connection line structure and said through connection region.

5. The device according to Claim 4, wherein said external connection structure (12-17) comprises an external pad region (12) extending on said first insulating layer (11) and a metal connection region (15) extending inside said insulating layer and having a first end in direct electrical contact with said external connection region and a second end in direct electrical contact with said first contact region (17).

6. The device according to Claim 5, wherein said through connection region (22) has an elongated shape extending on said metal connection region (15), and said through insulating region (23-25) is substantially U-shaped.

7. The device according to Claim 6, wherein said through insulating region (23-25) comprises a semicircular portion (23a-25a) partially surrounding said through connection region (22) and a pair of rectilinear portions (23b-25b) extending from said semicircular portion as far as a side edge of said third chip (5) outside said metal connection region (15) in top view.

8. The device according to any of Claims 1 to 3, further comprising a capacitive element (50) formed between said through connection region (43) and low-voltage electronic components (7).

9. The device according to Claim 2 or Claim 3, wherein said through region (44-46) has a cylindrical tubular shape.

10. The device according to Claim 9, wherein said first chip (4) comprises a first substrate (10) of semiconductor material; a first insulating layer (11) on top of said first substrate; an electronic component (7) formed at least partially in said first substrate; a second metal line structure (40) formed inside said first insulating layer and connected between said electronic component and a third contact region (41) formed on top of said first insulating layer and in electrical contact with said first semiconductor region (48); and wherein said second chip (6) comprises a second substrate (33) of semiconductor material; a second insulating layer (32) on top of said second substrate; and a third metal line structure (52) formed inside said second insulating layer and comprising a fourth contact region (51) extending between said second insulating layer and said through connection region (43).

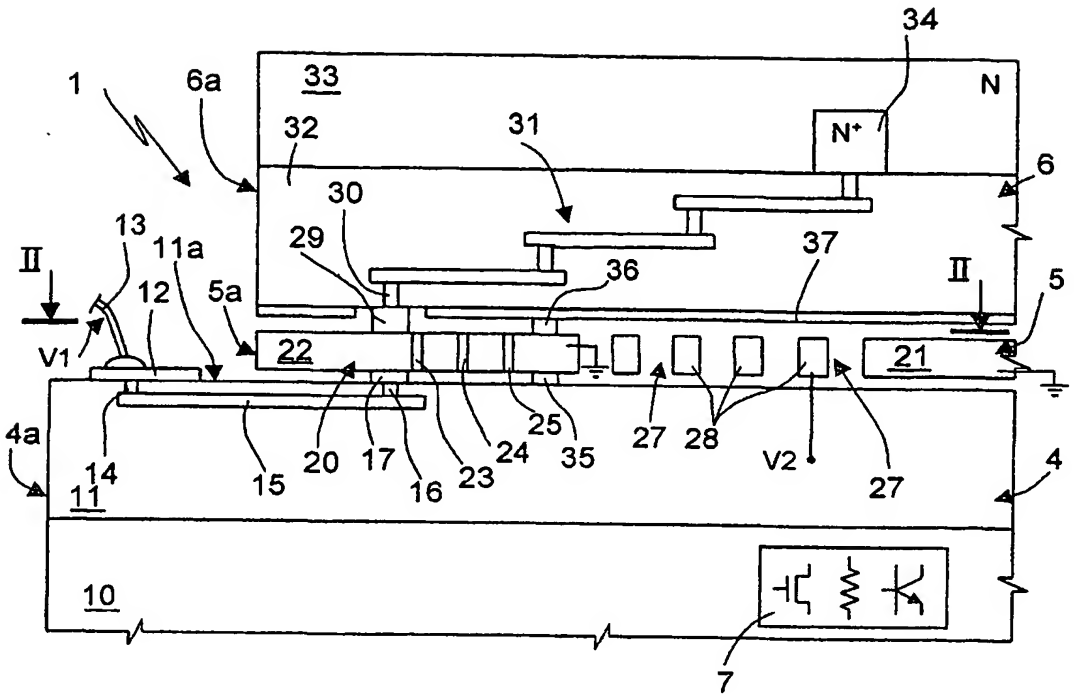
11. The device according to any of the foregoing claims, further comprising a shield structure (70) extending between said second chip (6) and said third chip (5).

12. The device according to Claim 11, wherein said shield structure (70) comprises a dielectric layer (71) extending on a face of said second chip (6) facing said third chip (5), and a conductive layer (72) covering said dielectric layer and facing said third chip.

13. The device according to Claim 12, wherein said conductive layer (72) is electrically connected to said low-voltage region (21).

14. The device according to Claim 12 or Claim 13, wherein electrical connection regions (73) of conductive material extend between, and are in electrical contact with, said conductive layer (72) and said low-voltage region (21).

15. The device according to any of Claims 12 to 14, wherein said dielectric layer (71) is a polyimide layer.


34
1
6a
33
N
32
31
N+
6
30
13
11a
29
37
II
36
II
5
12
5a
V1
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4a
14
15
20
17
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23
24
25
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Fig.1

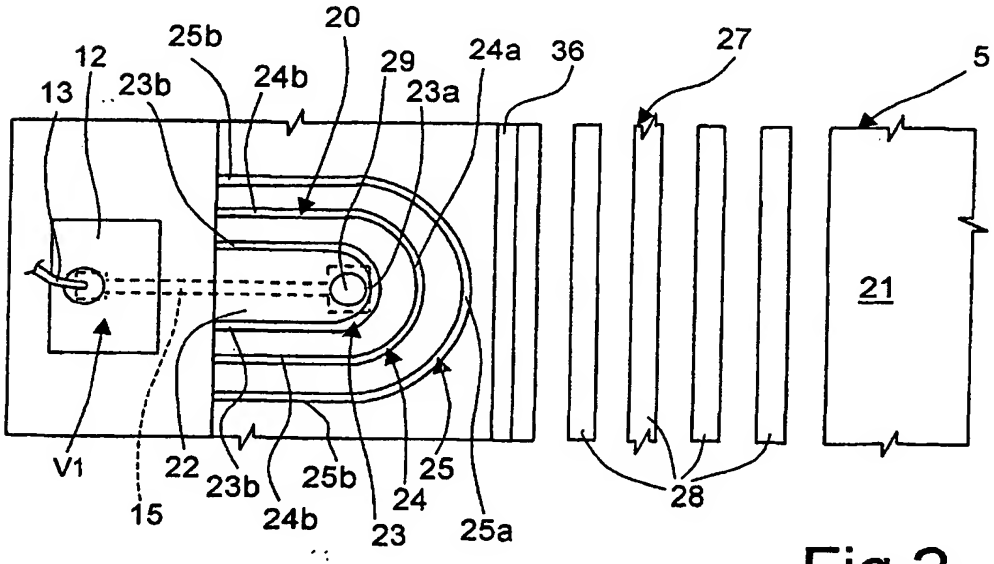
20
25b
12
24b
29
24a
36
27
5
13
23b
23a
21
V1
22
23b
25b
25
24
28
15
24b
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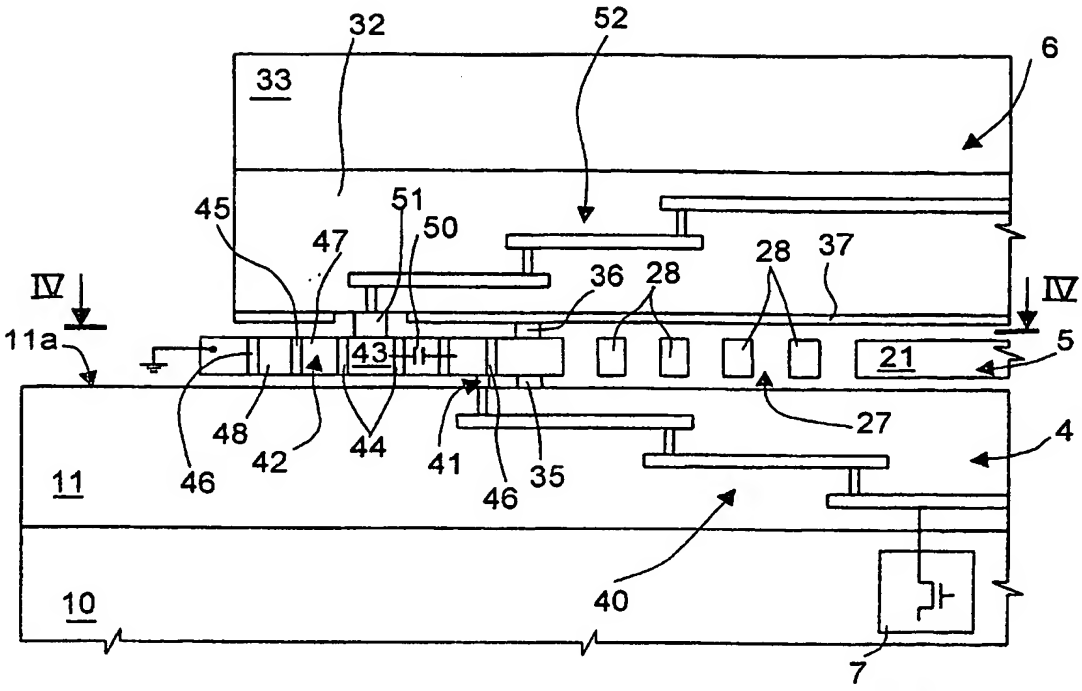
Fig.2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43
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5
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42
44
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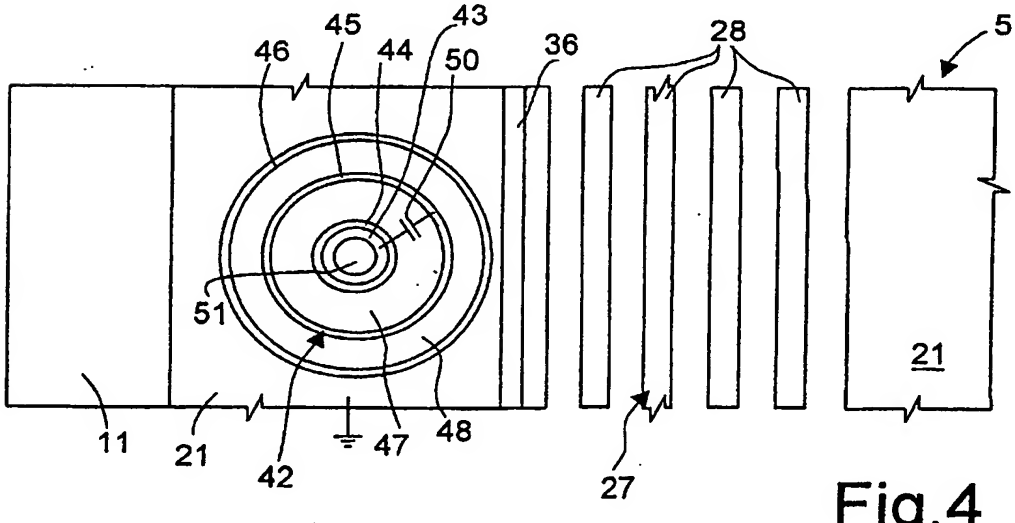
Fig.3


46
45
44
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50
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51
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42
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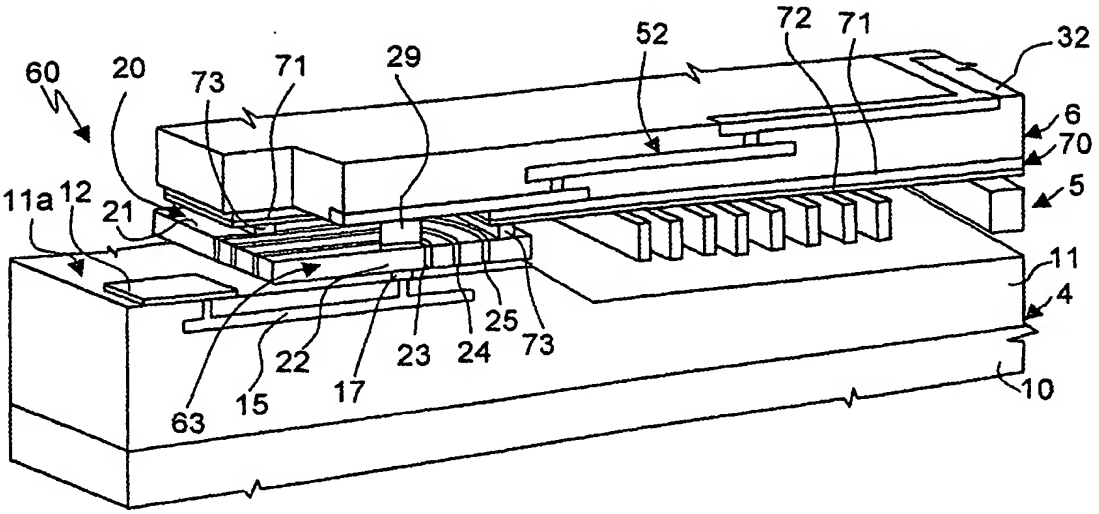
Fig.4


60
20
73
71
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52
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Fig.5

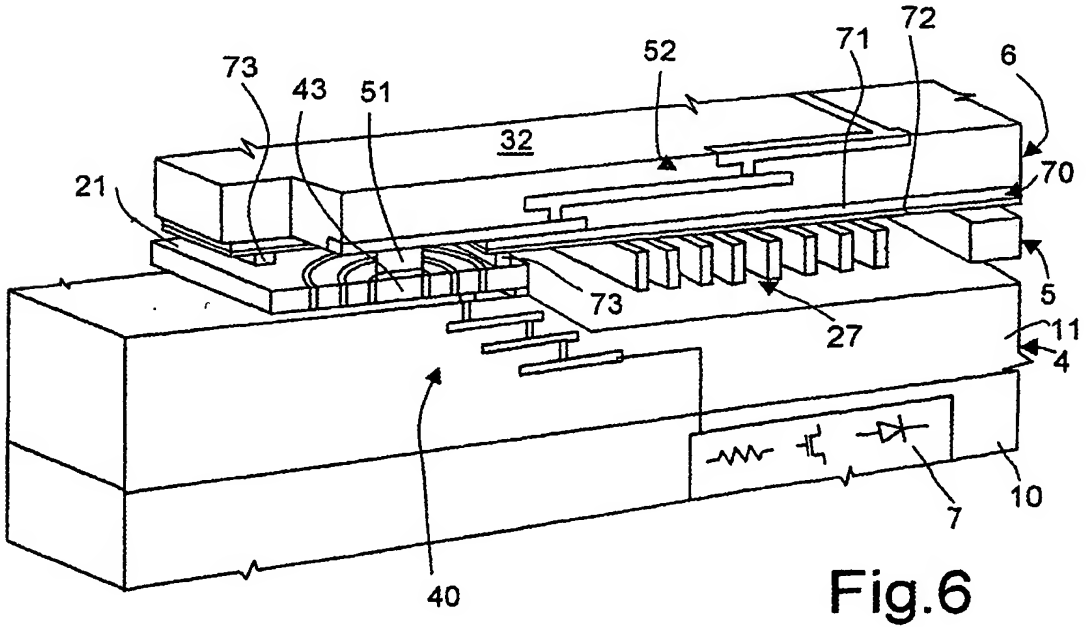
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Fig.6

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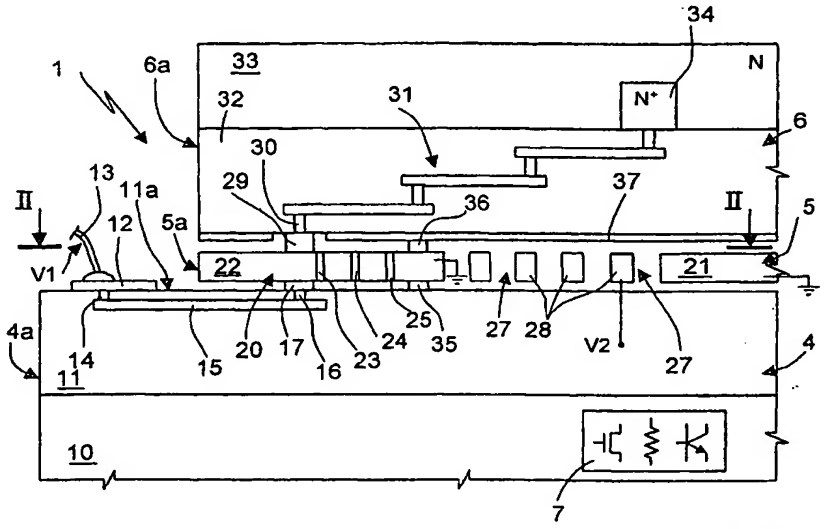

Fig.1

EP 1 225 635 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 02 00 1501

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	DE 199 58 486 A (FRAUNHOFER GES FORSCHUNG) 7 December 2000 (2000-12-07)	1	H01L23/48 H01L25/16
A	* column 5, line 22 - column 6, line 23; figure 4 *	2-15	H01L25/065 H01L25/07 B81C3/00
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Place of search	Date of completion of the search	Examiner
MUNICH	20 May 2003	Edmeades, M

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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